STIC Search Report
EIC 2800

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STIC Database Tracking Number: 126113

TO: David Hogans **Location: JEF 7D58** **Art Unit : 2813** **Friday, July 09, 2004** **Case Serial Number: 09/683857**	**From: Scott Hertzog** **Location: EIC 2800** **JEF4B68** **Phone: 272-2663** **Scott.hertzog@uspto.gov**

Search Notes

Examiner Hogans,

Attached are edited first pass search results from the patent and nonpatent databases.

Colored tags indicate abstracts especially worth your review.

If you need further searching or have questions or comments, please let me know.

Thanks,
Scott Hertzog

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Search and Information Resources Administration

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         (c) 1999 Electric Power Research Inst.Inc
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 647:CMP  Computer Fulltext 1988-2004/Jun W4
         (c) 2004 CMP Media, LLC

Set     Items   Description
S1       1927   ((LOW OR LOWER)(2N) (VOLT???? OR EMF OR POTENTIAL OR
                  THRESH????))(3N)(WELL? OR HOLE? ? OR SHAFT? ?)
S2       1641   ((HIGH OR HIGHER)(2N) (VOLT???? OR EMF OR POTENTIAL OR
                  THRESH????))(3N)(WELL? OR HOLE? ? OR SHAFT? ?)
S3      21705   (SECOND OR ADDN??? OR ADDITIONAL OR SUPPLEMENT???)(5N)(OXIDE? OR
                  DIELECTRIC OR SIO2 OR (SIO(W)2) OR SI3N4 OR (SI(W)3(W)N(W)4) OR SIN
                  OR SILICA OR (SI OR SILICON)(2N)(DIOXIDE? OR NITRIDE OR O OR O2 OR N
                  OR N4) OR PASSIV???? OR PROTECT????)
S4    4316631   HOLE? ? OR WINDOW??? OR OPEN???? OR ETCH? OR RIE OR REMOV???? OR
                  EXPOS???
S5    1488280   DOPANT? ? OR IMPURIT? OR IMPREGNAT? OR ADDITIVE? ? OR IMPLANT?
S6   17938734   METHOD? ? OR PROCESS??? OR FABRICAT????
S7          0   S1 AND S2 AND S3 AND S4 AND S5 AND S6
S8          0   S1 AND S2 AND S3 AND S4 AND S5
S9         98   S1 AND S2
S10         1   S1 AND S2 AND S3
S11        16   S1 AND S2 AND S4
S12        16   S1 AND S2 AND S4 NOT S10
S13         9   S1 AND S2 AND S4 NOT S10 AND (S3 OR S5:S6)
S14         7   RD (unique items)
S15         7   S12 NOT S13
S16         6   RD (unique items)
S17         5   S16 NOT PY>2002
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13/9/6 (Item 2 from file: 8)
DIALOG(R)File 8:**Ei Compendex(R)**

05192750 E.I. No: EIP98124511635
Title: Reduction of substrate-induced gate lag in GaAs MESFET's
Author: Bao, Jianwen; Leoni, Robert E. III; Du, Xiaohang; Hwang, James C.M.; Shah, Divyang M.; Jones, J. Robert; Shokrani, Mohsen L.
Corporate Source: Lehigh Univ, Bethlehem, PA, USA
Conference Title: Proceedings of the 1998 20th Annual IEEE Gallium Arsenide Integrated Circuit Symposium
Conference Location: Atlanta, GA, USA Conference Date: 19981101-19981104
Sponsor: IEEE
E.I. Conference No.: 49405
Source: Technical Digest - GaAs IC Symposium (Gallium Arsenide Integrated Circuit) 1998. IEEE, Piscataway, NJ, USA,98CH36260. p 103-106
Publication Year: 1998
CODEN: TDGSEE
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 9902W3
Abstract: **Methods** to suppress substrate trap-induced gate lag in ion-**implanted** GaAs MESFET's have been investigated in detail. It was found that the **methods** generally involve a supply of **holes** which can combine with the trapped electrons which are the culprits of gate lag. For high-power amplifiers employing **high** drain **voltages, holes** can be supplied through impact ionization. For battery-operated amplifiers employing **low** drain **voltages, holes** can be supplied through a contact to the buried p-layer. (Author abstract) 6 Refs.
Descriptors: MESFET devices; Semiconducting gallium arsenide; Ion **implantation**; Impact ionization; Power amplifiers; Substrates; Electrons; Electric potential; Gates (transistor)
Identifiers: Gate lag; Drain voltages
Classification Codes:
712.1.2 (Compound Semiconducting Materials)
714.2 (Semiconductor Devices & Integrated Circuits); 712.1 (Semiconducting Materials); 802.2 (Chemical Reactions); 713.1 (Amplifiers)
714 (Electronic Components); 712 (Electronic & Thermionic Materials); 802 (Chemical Apparatus & Plants); 713 (Electronic Circuits); 801 (Chemical Analysis & Physical Chemistry)
71 (ELECTRONICS & COMMUNICATIONS); 80 (CHEMICAL ENGINEERING)

13/9/9 (Item 1 from file: 647)
DIALOG(R)File 647:**CMP Computer Fulltext**

STM polishes mixed **processes**
Martin Gold
ELECTRONIC ENGINEERING TIMES, **1996**, n 902, PG18
PUBLICATION DATE: 960520
Agrate Brianza, Italy - To protect its base in power semiconductors and broaden its position in mixed-technology devices, SGS-Thomson

Microelectronics (STM) has launched several submicron **processes** and developed new architectures.

No fewer than five 8-inch wafer fabs will provide the capacity to support new devices resulting from the technology thrust. Included is a fab coming on stream in the fourth quarter for non-volatile memories and another planned for later in the decade.

The centerpiece of the technology arsenal is a new submicron generation of the company's bipolar/CMOS/DMOS **process**. The BCD5, in 0.6-micron lithography, integrates power functionality with memory, microcontroller and a DSP core on one chip. The **process** is aimed at applications in harsh environments, such as automotive engine control , ink-jet printers and power supplies.

Complementing BCD5 is another new **process**, CD5, in which the bipolar portion is eliminated for cost-sensitive applications.

"These **processes** bring power technology into the realm of VLSI," Bruno Murari, R&D director of the company's dedicated products group , told the U.S. and European press during recent briefings here and in Catania, Italy.

What's more, the company has enhanced its capabilities in power MOSFETs and RF bipolar for such applications as electronic-lighting systems and telecommunications basestations. Working with the University of Catania, SGS-Thomson is developing a silicon-germanium- based **process** as an alternative to gallium-arsenide for telecommunications. And a major effort is under way to develop and market application-specific discretes. Multiple power-discrete functions are being integrated into a single chip solution.

Key investment

The investment in new **processes** and in 8-inch-wafer fabs is essential if the company is to maintain its position in power-semiconductor technology, said Pasquale Pistorio, SGS-Thomson's president and chief executive officer. He stressed that the company is committed to adding fab capacity during the next few years despite "some market correction" currently affecting semiconductors.

Officials of the dedicated products group-which now accounts for more than half of the company's approximately $4 billion in annual sales-touted applications for the BCD5 and CD5 **processes**, which are based on 0.6-micron CMOS lithography. The BCD3 predecessor to BCD5 is based on 1.2-micron lithography. The pulsewidth modulator, voice coil and spindle block in a hard-disk drive are among the targeted applications for BCD5.

"The importance of BCD5 is that it combines power functions on a standard CMOS/VLSI platform with no changes in substrate," said Claudio Contiero, new-**processes** design manager for the dedicated- products operation. Compatibility between power functions and the VLSI-**process** platforms is achieved via a scheme that exploits a large -angle tilt **implant** to develop a power LDMOS region without the need for extra thermal steps.

The CMOS operating voltage is 5 V. Breakdown voltages are specified in the 16- to 40-V range. However, the voltage level can be extended to 80 V.

Among the features of BCD5 are its n-type epitaxial layer on a p-type substrate and its use of twin-well CMOS. Different n-**wells** address **low**- and **high-voltage** power LDMOS. The **process** also uses two thin interconnect metal layers and another level that's either a thin - or thick-metal interconnect. Gate-oxide thickness is specified at 200/330 microns; tunnel oxide thickness is 70

microns. There is a single polycide gate on the differential gate oxide.

Devices based on BCD5 and CD5 are scheduled to be available in small quantities in the first half of 1997; volume production will start in the second.

Meanwhile, work has started on the 0.35-micron-lithography BCD6. Target applications include hard disk drives.

For the next generation of both its high- and low-voltage power-MOSFET lines, SGS-Thomson has developed an architecture that replaces the conventional cell structure used in power MOS with a structure that takes the form of a strip.

"Packing density is limited in the older architecture," noted Ian Wilson, the company's power-transistor product manager. The three- strip structure triples the packing density, Wilson said.

In the strip architecture, there is no p+ mask, no contact mask and no need for source alignment. The architecture enables a die-size reduction of greater than 20 percent and an epitaxial thickness reduction of greater than 12 percent. The minimum size of the strip is 1.2 microns, according to Wilson.

The patent-pending strip layout, coupled with the company's proprietary edge-termination structure, provides a much lower Rds(on) per unit of area and improvements in avalanche and dv/dt capabilities, as well as in gate-charge and switching capabilities. Typical Rds(on) is 0.33 ohms . Typical gate-to-source voltage rating is +/- 30V. High-voltage MOSFETs with the strip architecture employ a 3-D mesh overlay structure.

The strip architecture will also be applied to the company's insulated-gate bipolar-transistor line.

Switch-mode target

The strip architecture is aimed at switch-mode power supplies, automotive electronic ignition, dc/ac converters for welding equipment , uninterruptible power supplies and motor drives. Devices for switch -mode power supplies deliver 15 A or 20 A at voltages as high as 500 V. Sampling of high-voltage devices based on the architecture began recently, with low-voltage devices expected to be available at yearend.

For its newest high-speed bipolar (HSB) RF **processes**, SGS-Thomson is looking at 900-MHz GSM radio front ends, 1.8-GHz DCS front-end blocks, a CT2 digital cordless single-chip radio and DECT (digital enhanced cordless telephones). The HSB2A offers an Ft of 20 GHz, a propagation delay of 30 ps and an early voltage rating of greater than 30 V.

Already in development is the next-generation HSB3. Based on having 0.2-micron polysilicon emitters available, the **process** hopes to deliver an Ft of close to 50 GHz. The most likely application will be the new multimode 900-MHz GSM, 1.8-GHz PCN and 1.9-GHz PCS-based systems. The company also is evaluating the integration of HSB3 and silicon-germanium **processes** to achieve higher integration and low power.

Also on SGS-Thomson's technology agenda is its application-specific discretes (ASDs). The devices combine multiple discrete device functions on one chip. A cell library that includes transistors, thyristors, Schottky diodes and zeners has been developed and is available for ASDs. CAD tools are similar to those used in developing conventional ASICs. Initially, SGS-Thomson will do the design; later, customers will design and develop their own ASDs. Design centers will be **opened** worldwide.

File 348:**EUROPEAN PATENTSEUROPEAN PATENTS 1978-2004**/Jul W01
(c) 2004 European Patent Office
File 349:**PCT FULLTEXTPCT FULLTEXT 1979-2002**/UB=20040701,UT=20040624
(c) 2004 WIPO/Univentio

Set	Items	Description
S1	877	((LOW OR LOWER)(2N) (VOLT???? OR EMF OR POTENTIAL OR THRESH????))(3N)(WELL? ? OR HOLE? ? OR SHAFT? ?)
S2	1219	((HIGH OR HIGHER)(2N) (VOLT???? OR EMF OR POTENTIAL OR THRESH????))(3N)(WELL? ? OR HOLE? ? OR SHAFT? ?)
S3	58216	(SECOND OR ADDN??? OR ADDITIONAL OR SUPPLEMENT???)(5N)(OXIDE? OR DIELECTRIC OR SIO2 OR (SIO(W)2) OR SI3N4 OR (SI(W)3(W)N(W)4) OR SIN OR SILICA OR (SI OR SILICON)(2N)(DIOXIDE? OR NITRIDE OR O OR O2 OR N OR N4) OR PASSIV???? OR PROTECT????)
S4	1212139	HOLE? ? OR WINDOW??? OR OPEN???? OR ETCH????? OR RIE OR REMOV???? OR EXPOS???
S5	359096	DOPANT? ? OR IMPURIT? OR IMPREGNAT? OR ADDITIVE? ? OR IMPLANT?
S6	155	S1 AND S2 AND (METHOD? ? OR PROCESS??? OR FABRICAT???? OR -MAKE OR MADE OR MAKING)
S7	30	S1 AND S2 AND S3 AND S4 AND S5 AND S6
S8	30	IDPAT (sorted in duplicate/non-duplicate order)
S9	**27**	**IDPAT (primary/non-duplicate records only)**

9/TI,PN,AU,IN,PD,AN,AD,AB,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:**EUROPEAN PATENTS**(c) 2004 European Patent Office. All rts. reserv.

Systems and **methods** for integration of heterogeneous circuit devices
Systeme und Verfahren zur Integration von heterogenen Schaltkreis-Bauelementen
Systemes et procedes pour l'integration de dispositifs circuits heterogenes
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PATENT (CC, No, Kind, Date): EP 1339101 A2 030827 (Basic)
APPLICATION (CC, No, Date): EP 2003003955 030221;
PRIORITY (CC, No, Date): US **683857** 020222

ABSTRACT EP 1339101 A2
A heterogeneous device comprises a substrate and a plurality of heterogeneous circuit devices defined in the substrate. In embodiments, a plurality of heterogeneous circuit devices are integrated by successively masking and ion **implanting** the substrate. The heterogeneous device may further comprise at least one microelectromechanical system-based element and/or at least one photodiode. In embodiments, the heterogeneous circuit devices comprise at least one CMOS transistor and at least one DMOS transistor. In embodiments, the substrate comprises a layer of silicon or a layer of p-type silicon. In other embodiments, the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer or a single-crystal-P-silicon layer, a substrate and an insulator layer therebetween.

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:**EUROPEAN PATENTS**(c) 2004 European Patent Office. All rts. reserv.

Semiconductor device having NMOS and PMOS transistors on common substrate and **method** of **fabricating** the same
INVENTOR:
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PATENT (CC, No, Kind, Date): **EP 849801 A2 980624** (Basic)
EP 849801 A3 980923
APPLICATION (CC, No, Date): EP 97122323 971217;
PRIORITY (CC, No, Date): JP 96340694 961220

ABSTRACT EP 849801 A2
There is provided a **method** of **fabricating** a semiconductor device, comprising the steps, in order, of, forming first well regions (105A, 105B, 105C, 105D) in a semiconductor substrate (101, 201) in all regions in which high-voltage and low-voltage MOS transistors (51, 52, 53, 54) are to be formed, the semiconductor substrate having a first conductivity and the first well regions having a second conductivity, forming an isolation layer (109) for isolating the first well regions from each other, forming **high-voltage well** regions (110A, 110B) having a first conductivity, and **low-voltage well** regions (110C, 110D) having first and second conductivity, and forming MOS transistors on the **high-voltage** and **low-voltage well** regions. The **high-voltage** and

low-voltage well regions are formed with the isolation layer being used as a mark. The **method** makes it possible to form low-voltage and high-voltage MOS transistors on a common semiconductor substrate in the smallest number of **fabrication** steps.

...on the p-type silicon substrate 401, followed by deposition a photoresist film 403 all over the oxide film 402. Then, a first photolithography and **etching** step is carried out to thereby partially **remove** the oxide film 402 in regions where high-**voltage** and **low-voltage** n-type **well** regions are to be formed, with the photoresist film 403 being used as an **etching** mask.

Then, as illustrated in Fig. 2B, after the photoresist film 403 has been **removed**, a thin oxide film 491 is grown on a surface of the p-type silicon substrate 401 in **exposed** regions thereof. The oxide film 491 has a thickness of about 40 nm. The oxide film 491 is grown for preventing channeling in ion-**implantation** and precipitation of **impurities** caused by thermal annealing carried out at a high temperature. Then, the p-type silicon substrate 1 is **implanted** at 150 KeV with doses of 1 X 1013) cm-2) of n-type **impurity** ions such as phosphorus with the oxide film 402 being used as an ion-**implantation** mask. Thus, there are formed ion-**implanted** regions 404A, 404B and 404D.

Then, a first annealing is carried out at 1200(degree)C for about 5 hours. As a result, the ion-**implanted** regions or n-type **impurity** regions 404A, 404B and 404D are diffused laterally and in a depth-wise direction of the p-type silicon substrate 401 to thereby **make impurity** regions 405A, 405B and 405D, as illustrated in Fig. 2C. The oxide film 491 is all **removed**, and then a thin oxide film 492 is formed again at a surface of the p-type silicon substrate 401.

Then, a photoresist film 403 is formed again entirely over the **oxide** film 492. Then, a **second** lithography step is carried out to the photoresist film 403 employing an alignment mark having been formed in the first lithography step, to thereby pattern the photoresist film 403 into a desired pattern. Then, p-type **impurities** are ion-**implanted** into the n-type well region 405B in a selected area with the patterned photoresist film 403 being used as a mask, to thereby form an **impurity** region 406B in the n-type well region 405B, as illustrated in Fig. 2D. The thus formed **impurity** region 406 will **make** a **high-voltage** p-type **well** for the **high-voltage** PMOS transistor.

Then, as illustrated in Fig. 2E, a nitride film 407 is grown on the oxide film 492 by a thickness in the range...

...all over the nitride film 407, followed by a third photolithography step to thereby pattern the photoresist film 403. Then, the nitride film 407 is **etched** for **removal** in selected regions where device isolation regions are to be formed, with the patterned photoresist film 403 being used as a mask. After **removal** of all the photoresist film 403, the product is oxidized at 1000(degree)C to 1200(degree)C for about 3 hours. This oxidation doubles...

...oxide films 410 have a thickness in the range of about 50 nm to about 70 nm. By the above-mentioned oxidation, the n-type **impurity** regions

405A, 405B and 405D, and the p-type **impurity** region 406B are diffused laterally and in a depth-wise direction of the silicon substrate 401 to thereby **make** n-type **impurity** regions 408A, 408B and 408D, and the p-type **impurity** region 409B, respectively.

The steps mentioned so far are a known **method** called LOCOS for defining device formation regions. LOPOS or trench type LOCOS may be substituted for LOCOS, in which case, a distance Xn2 (see Fig. 2F) between the oxide film 410 and an outer boundary of the n-type **impurity** region 408A varies in dependence on a target breakdown voltage of the high-voltage NMOS transistor, and further a distance Xp2 (see Fig. 2F) between the oxide film 410 and an outer boundary of the p-type **impurity** region 409B varies in dependence on a target breakdown voltage of the high-voltage PMOS transistor. The distances Xn2 and Xp2 are dependent on the...

...is determined in a complicated manner. That is, the distance Xn3 is dependent on the lateral diffusion of the region 404A, into which n-type **impurities** have been **implanted** in Fig. 2B, caused by two high temperature thermal annealing. The distance Xp3 in the high-voltage PMOS transistor is determined in a more complicated manner. The region 406B having been formed by **implanting** p-type **impurities** thereinto with the oxide film 402 being used as an alignment mark is laterally diffused by the first high temperature annealing to thereby **make** the **high-voltage** p-type **well** region 409B illustrated in Fig. 2L. Apart from the **high-voltage** p-type **well** region 409B, the device isolation oxide film 410 is formed also with the oxide film 402 being used as an alignment mark. Namely, the distance Xp2 between the device isolation oxide film 410 and an outer end of the **high-voltage** p-type **well** region 409B is formed under the influence of both a dispersion caused by two photolithography steps and a dispersion caused by a high temperature thermal...

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/8 (Item 8 from file: 348)

DIALOG(R)File 348:**EUROPEAN PATENTS**

High withstand voltage M I S field effect transistor and semiconductor integrated circuit

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Fujishima, Naoto, Fuji Electric Co., Ltd., 1-1, Tanabeshinden, Kawasaki-ku, Kawasaki-shi, Kanagawa, (JP)

PATENT (CC, No, Kind, Date): EP 805499 A2 971105 (Basic)
EP 805499 B1 020508

APPLICATION (CC, No, Date): EP 97111861 930812;

PRIORITY (CC, No, Date): JP 92217705 920817; JP 92309920 921119

ABSTRACT EP 805499 A3

A high withstand voltage M I S field effect transistor having a second conductivity type will region (2) formed on a first conductivity type semiconductor substrate (1); an M I S portion (25) providing in a first edge portion of the well region (2) a first conductivity type base layer (3), a second conducting type source layer (8) formed in the base layer (3) and a gate electrode (7) disposed through an insulating gate film (6)

over the source layer (8) and an area of said well region (2); a drain portion (26) providing a second conductivity type drain layer (9) formed in a second edge portion of said well region (2); a first conductivity type offset region (42) formed in said well region between said MIS portion (25) and said drain portion (26), wherein at least one portion of said offset region (42) is formed under said gate electrode (7); and at lest one conducting layer (41) disposed through an insulating film (6) over said offset region (42).

...SPECIFICATION

...a continued well region extended to a drain layer in a lateral direction and by providing in the transistor a second base region on the **well** region. The **high** withstand **voltage** MIS field effect transistor has a second conducting type well region formed on a first conducting type semiconductor substrate; a MIS portion has a pair...
...to the source layer, it is preferable to use a field plate type source electrode extended by about 5 micrometers or more onto the field **oxide** film on the **second** base layer. As a drain electrode connected to the drain layer, it is preferable to use a field plate type drain electrode extended by about 5 micrometers or more onto the field **oxide** film on the **second** base layer. Further, the **impurity** concentration of the second base layer is effectively lower than the **impurity** concentration of the first base layer.
As a flat structure of such high withstand voltage MIS field effect transistor, it is preferable that the second...

...be substantially concentrically formed with respect to the drain layer as a center. The second base layer may provide at least one portion which is **exposed** for the field oxide film.
As a means for actively decreasing influence by the field oxide film and forming a high withstand voltage element, it...

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:**EUROPEAN PATENTS**

Improvements in or relating to integrated circuits
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Lattaro, Cristina, Avezzano, Aquila, (IT)
PATENT (CC, No, Kind, Date): EP 768673 A2 970416 (Basic)
EP 768673 A3 980930
APPLICATION (CC, No, Date): EP 96305290 960718;
PRIORITY (CC, No, Date): US 1507 950719

ABSTRACT EP 768673 A2
A **method** for selectively erasing one or more non-volatile programmable memory cells in an integrated circuit. The **method** is applicable to an array 1 of memory cells 10 **fabricated** in a semiconductor substrate 30 of a first conductivity type semiconductor

material, each cell having a floating gate 14 for programming the cell and a control gate 11 for reading the cell, the array having a plurality of row lines 15, a plurality of column lines 25 and a plurality of output lines 18. The cells should be formed in a first well 33 of said first conductivity type semiconductor material, the first wells being formed in second wells 31 of a second conductivity type semiconductor material, the first wells including cells in groups of one or more. The **method** involves the steps of applying a high voltage source to a selected one or more column lines, applying a zero voltage source to a selected one or more row lines; and applying the high voltage source to non-selected row lines. The **method** is particularly suited to Flash memories. Erasure can be sectored by grouping cells in separate ones of the first wells and applying the **method** selectably to such groups.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Process Overview

The **process** used in the manufacture of the preferred embodiment includes forming a floating-gate cell, a line of such cells, or an array of such cells...

...equal to the first positive voltage, thus eliminating the field-plate breakdown-voltage problem. Because there is no need for a diffused source-junction erase **window** under the floating gate, each floating-gate cell is a one-transistor cell having roughly the same area as that of an ultra-violet-erasable EPROM cell **made** using the same technology. Without the prior-art requirement for a separate tunnelling region near the source, a masking step and a phosphorus **implant** are eliminated. The preferred embodiment is realized in an X-cell memory array that has the small size of an ultra-violet-erasable EPROM and...

...wells", "tanks" or "tubs". The "wells", "tanks" or "tubs" are generally large enough to contain the diffusion regions and channels of active circuit elements.

The **process** results in a memory array with rows and columns of cells having a size and structure similar to those of a prior-art ultra-violet...

PROCESS DETAILS

Referring now to FIG. 1, a memory device is shown which has an Array 1 of rows and columns of memory cells 10, each...wells 31 (see FIG. 2) are programmed and erased with the P-wells 33 and N-wells 31 at 0V.

Placing Array 1 in the **low** voltage P-**well** 33, with the **high voltage** N-**well** 31 encasing P-well 33, all in a P-type substrate 30, allows a novel electrical erase **method** for the Array 1, when Array 1 is comprised of Flash memory cells. In this mode, P-well 33 and N-well 31 are shorted...may be interchanged in the read example above.

For convenience, a table of read and write voltages is given in the Table 1 below:

A **method** of **making** the devices of FIG. 1 will be described in reference to FIGs. 2 and 3a-3k. The **method** description relates only to the **process** for forming an X-cell array of cells 10 and for forming both the high-voltage P-channel transistors HVPT and low-voltage N-channel...

The above steps correspond to those described in conjunction with the text describing Figures 3(a)-3(k). By way of clarification, however, note the following. ALIGN(underscore)0 is a conventional initial alignment step; HV(underscore)NWELL is the step of formation of Deep N-**wells** 31 for **high voltage** p-channel devices; HV(underscore)PWELL is the step of formation of P-**wells** for **high voltage** n-channel devices which, it will be recalled is not described hereinabove, but which is a well known **process** step; LV(underscore)NWELL is the step of formation of N-**wells** for **low voltage** p-channel devices, also not described hereinabove, but also a well known **process** step ; LV(underscore)PWELL is the step of formation of P-**wells** 33 for **low voltage** n-channel devices and the memory array p-well; MOAT is the step of creating the isolation regions 41 of oxide; C/S is the step of formation of the channel stops; ARRAY VT is the step of threshold-voltage-adjust **implant** in the memory array; POLY1 is the step of defining the first polysilicon layer outside the memory array; SLIT is the step of **removing** the strips that define the ends of the floating gates; LVPVT is the **implantation** step by which the low voltage p-channel device threshold voltage is determined; LVNVT is the **implantation** step by which the low voltage n-channel device threshold voltage is determined; ROM(underscore)VT is a patterened **implantation** step by which the threshold voltage for selected bits in the ROM array is determined; POLY2 is the step of defining the second polysilicon layer; STAC is the step by which the control and floating gates are formed by **etching**; ARRAY(underscore)SD is an **implant** step by which the memory array sources and drains are formed; NSD is the step by which the n-channel source drain regions are formed...

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/10 (Item 10 from file: 348)

DIALOG(R)File 348:**EUROPEAN PATENTS**(c) 2004 European Patent Office. All rts. reserv.

Semiconductor device

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PATENT (CC, No, Kind, Date): EP 721211 A2 960710 (Basic)
EP 721211 A3 961227
EP 721211 B1 031203

APPLICATION (CC, No, Date): EP 96104114 890206;

PRIORITY (CC, No, Date): JP 8826787 880208; JP 88246441 880930

ABSTRACT EP 721211 A3

A semiconductor device includes a semiconductor substrate, a pair of low breakdown voltage elements formed in the substrate so as to be adjacent to each other, and a high breakdown voltage element formed to be adjacent to one of the low breakdown voltage elements. The pair of low breakdown voltage elements are isolated from each other by a pn junction and the one of the low breakdown voltage elements and the high breakdown voltage element are isolated from each other by a dielectric material. The semiconductor substrate is a composite substrate formed by

directly bonding a first substrate serving as an element region to a second substrate serving as a supporting member through an insulating film. (see image in original document)

...a semiconductor device in which low breakdown voltage elements are formed in two wells having V-shaped sectional areas. In the above-described embodiments, the **method** of forming a trench and burying a semiconductor layer therein, and the **method** of **impurity** diffusion are described as **methods** of forming wells isolated by pn junction isolation. The **method** of forming trenches described with reference to Figs. 2A to 2G is performed independently of the selective **etching process** for forming island Si layers by isolation. In this embodiment, however, trenches are formed in the wells simultaneously with the selective **etching process** for isolation of the island Si layers. The trenches for isolating/forming the island layers must reach the bottom portions while the trenches in the well regions must not reach the bottom portions. Such conditions can be obtained by applying anisotropic **etching** capable of obtaining a predetermined taper angle to selective **etching** so as to select the size of an **etching window.**

Figs. 12A to 12G are sectional views showing the steps in manufacturing the semiconductor device in Fig. 11. The steps shown in Figs. 12A and...

...element side and Si layer 4b on the low breakdown voltage element side are isolated from each other by forming isolation trench 32 by selective **etching**. At the same time, trenches 32a and 32b are formed in the **well** regions on the **low** breakdown **voltage** element side (Fig. 12C). By selecting the size of a **window** of SiO(sub(2)) upon anisotropic **etching**, trench 32 of the isolation region can be caused to reach the bottom portion while trenches 32a and 32b in the well regions do not...

...simultaneously integrated as pnp transistors.

In the embodiments shown in Figs. 4 to 7, the same effects as in the previous embodiment can be obtained.

Fig. 8 shows a **structure** of still another embodiment. In this embodiment, space 91 is formed at a position of bonding interface **2** below the IGBT-T1 region serving as the high breakdown voltage element in Fig. 1. This structure is obtained by forming oxide film 3a to a sufficient thickness by a **process** prior to bonding, **etching** oxide film 3a in the **high** breakdown **voltage** element region, forming **thin** oxide film 3c in the **etched** portion again, and performing bonding. **With** this structure, a breakdown voltage in a bottom portion of the high **breakdown** voltage **element** side can be further **increased.**

Fig. 9 is a sectional view of a semiconductor **device** in which low breakdown voltage elements are formed in two wells having V-shaped sectional areas. In **the above**-described embodiments, the **method** of forming a trench and burying a semiconductor layer therein, and the **method** of **impurity** diffusion are **described as methods** of forming wells isolated by pn junction isolation. The **method** of forming trenches described with reference to Figs. 2A to 2G is performed independently of the selective **etching process** for forming island Si layers by isolation. In this embodiment, however, **trenches** are formed in the wells

simultaneously with the selective **etching process** for isolation of the island Si layers. **The trenches** for isolating/forming the island layers must reach the bottom portions while the trenches in the well regions must not reach the bottom portions. Such conditions can be obtained by applying anisotropic **etching** capable of obtaining a predetermined taper angle to selective **etching** so as to select the size of an **etching window**.

Figs. 10A to 10G are sectional views showing the steps in manufacturing the semiconductor device in **Fig**. 9. The steps shown in Figs. 10A and 10B are the same **as** those in Figs. **2A** and **2B**. Si layer 4a on the high breakdown voltage element side **and** Si layer 4b on **the** low breakdown voltage element side are isolated from each other by forming isolation trench 32 by selective **etching**. At the same time, trenches 32a and 32b are formed in the **well** regions on the **low** breakdown **voltage** element side (Fig. 10C). By selecting the size of a **window** of SiO2)) upon anisotropic **etching**, trench 32 of the isolation region can be caused to reach the bottom portion while trenches 32a and 32b in the well regions do not reach the **bottom** portions. Thereafter, n+)-type layers 6c, 21a, and 21b are formed in the side walls of trenches 32, 32a, and 32b upon diffusion of phosphorus...

...by epitaxial diffusion (Fig. 10D). Similar to the embodiment shown in Figs. 2A to 2G, high-resistance n-)-type Si layer 22 is formed by **removing** an **oxide** film on the **low** breakdown **voltage** element side and forming an Si layer by epitaxial growth. At the same time, polysilicon layer 5 is deposited on the **high** breakdown voltage element covered with the oxide film (Fig. 10E). Then, the grown layer is lapped, n-)-type layers 22a and 22b serving as wells ...

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:**EUROPEAN PATENTS**(c) 2004 European Patent Office. All rts. reserv.

METHOD OF **FABRICATION** OF AN INTEGRATED CIRCUIT CHIP CONTAINING EEPROM AND CAPACITOR

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PATENT (CC, No, Kind, Date): EP 725980 A1 960814 (Basic)
EP 725980 B1 011205
WO 9607203 960307
APPLICATION (CC, No, Date): EP 95931647 950829; WO 95US11037 950829
PRIORITY (CC, No, Date): US 298239 940830

METHOD OF **FABRICATION** OF AN INTEGRATED CIRCUIT CHIP CONTAINING EEPROM AND CAPACITOR

...floating gate and positioned such that the floating gate extends laterally outwardly beyond the control gate around its entire periphery.

The invention also provides a **method** of **fabricating** a memory transistor in an EEPROM cell according to claim 2, the **method** comprising: providing a semiconductor substrate, depositing a first mask layer over the semiconductor member to define area for

source/drain regions of the memory transistor separated by a channel region **implanting dopant** to form the source/drain regions and **removing** the first mask; growing a gate **oxide** layer, depositing a **second** mask layer over the gate **oxide** layer to define an area for a tunnel oxide region overlying one of the source/drain regions, growing the tunnel **oxide** region and **removing** the **second** mask; depositing a first conductive layer over the gate oxide layer and tunnel oxide and an insulating layer over the first conductive layer, depositing a third mask layer to define an area for a floating gate of the memory transistor over the tunnel oxide, forming the floating gate and **removing** the third mask; depositing a second conductive layer over the insulating layer, forming a fourth mask to define areas for a control gate of the memory transistor over the floating gate, forming the control gate and **removing** the fourth mask, and in which the control gate is smaller than the floating gate and positioned so that the floating gate extends laterally outwardly beyond the control gate around its entire periphery.

The **process** of this invention may be used to **fabricate** an array of EEPROM cells and an array of interpoly capacitors on a conventional logic IC chip, preferably a chip containing conventional CMOS devices according...

...112 and N-wells 111 and 113 are formed in epitaxial layer 11. Field oxide regions 100, 101, 102, 103 and 104 and P- field **implant** regions 100P, 101P, 102P, 103P and 1034P are also formed by means of **processes** known in the art. Field oxide region 101 and P- field **implant** region 101P isolate P-well 110 from N-well 111, field oxide region 102 and P- field **implant** region 102P isolate N-well 111 from P-well 112, and field oxide region 103 and P- field **implant** region 103P isolate P-well 112 from N-**well** 113.

The relatively **high-voltage** NMOS devices of an EEPROM cell will be formed in P-well 110, and conventional (5 volts, 150 A gate thickness) CMOS devices will be formed in N-well 111 and P-**well** 112. An additional **high-voltage** PMOS device will be formed in N-well 113. A capacitor will be formed above field oxide region 104.

Referring further to Figs. 1A and 1B, following field oxidation a sacrificial gate oxide layer 120 is formed on the surface of the substrate. A threshold voltage adjust **implant** (represented by arrows 130) for the high-voltage devices to be formed within P-well 110 and N-well 113 is performed through sacrificial gate oxide layer 120. This **implant** is conducted without a mask and contains the entire dose necessary for setting the threshold **voltages** of the **high -voltage** devices within P-**well** 110 and N-**well** 113. The **high-voltage** devices will have gate oxides that are relatively thick (for example, 325 A). Threshold voltage adjust **implant** 130 also contains part of the **implant** dose that is required to adjust the threshold voltages of the low-voltage CMOS devices to be formed within N-well 111 and P-well 112.

Referring next to Figs. 2A and 2B, a first photoresist mask 140 is then applied to the surface of the substrate. An N-type **implant** 150 is performed through mask 140 to form source/drain regions 160, 161 and 162 within P-well 110. **Implant** 150 consists of two stages (phosphorus and arsenic **dopants**) so that source/drain regions 160, 161 and 162 are double-diffused, having an N+ region and a deeper surrounding N- region. **Implant** 150 may be performed with arsenic at a dosage of 1 x 1015) cm-2) and phosphorus at a dosage of 1 x 1014) cm-2).

The mask 140 and sacrificial gate oxide layer 120 are then **removed**. A gate oxide layer 165 is grown, as shown in Figs. 3A and 3B. Gate oxide layer 165 may be approximately 400 A thick but is somewhat thicker (for example, 600 A) over source/drain regions 160, 161 and 162. As shown in Figs. 4A and 4B, a **second**, tunnel **oxide** mask 170 is formed over all of gate oxide layer 165 except a portion thereof above source/drain region 161. A wet **etch** 180, using a buffered oxide **etch** (BOE), is then performed to **remove** the portion of oxide layer 165 which lies under the **opening** in mask 170. Mask 170 is then **removed** and, as shown in Figs. 5A and 5B, a tunnel oxide layer 190 is grown over the **exposed** portion of source/drain region 161. Tunnel oxide 190 is typically about 83 A thick and adds slightly to the thickness of oxide layer 165...

...CLAIMS smaller than the floating gate and positioned such that the floating gate extends laterally outwardly beyond the control gate around its entire periphery.

2. A **method** of **fabricating** a memory transistor (2) in an EEPROM cell, the **method** comprising:

providing a semiconductor substrate (10,11);

depositing a first mask layer (140) over the semiconductor substrate to define an area for source/drain regions (161,162) of the memory transistor separated by a channel region **implanting dopant** to form the source/drain regions and **removing** the first mask;

growing a gate **oxide** layer (165), depositing a **second** mask layer (170) over the gate oxide layer to define an area for a tunnel oxide region (190) overlying one of the source/drain regions (161), **removing** a portion of said gate **oxide** layer **exposed** by said **second** mask layer for growing the tunnel **oxide** region and **removing** the **second** mask;

depositing a first conductive layer (200) over the gate oxide layer and tunnel oxide and an insulating layer (210) over the first conductive layer...

...third mask layer (220) to define an area for a floating gate of the memory transistor over the tunnel oxide, forming the floating gate and **removing** the third mask;

depositing a second conductive layer (270) over the insulating layer, forming a fourth mask (280) to define areas for a control gate of the memory transistor over the floating gate, forming the control gate and **removing** the fourth mask, and in which the control gate is smaller than the floating gate and positioned so that the floating gate extends laterally outwardly beyond the control gate around its entire periphery.

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/13 (Item 13 from file: 348)

DIALOG(R)File 348:**EUROPEAN PATENTS**(c) 2004 European Patent Office. All rts. reserv.

High withstand voltage M I S field effect transistor and semiconductor integrated circuit

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PATENT (CC, No, Kind, Date): EP 588067 A2 940323 (Basic)
EP 588067 A3 940420
EP 588067 B1 990512
APPLICATION (CC, No, Date): EP 93112958 930812;
PRIORITY (CC, No, Date): JP 92217705 920817; JP 92309920 921119

ABSTRACT EP 588067 A2

A semiconductor integrated circuit device is provided in which a highly reliable and low cost intelligent power semiconductor is mounted on the same substrate as that of a control circuit having a logic element, such as a low withstand voltage C M O S etc., and a high withstand voltage and high current output M I S field effect transistor. A high withstand voltage M O S F E T is composed of a vertical M O S portion 25 formed in one side of a laterally widened well layer 2 and a drain portion formed in the other side thereof and a second base layer 4 is formed on the surface of the well layer 2. Accordingly, a depletion layer widened just under the M O S portion 25 and the second base layer 4 develops a J F E T effect at OFF time thereby realizing a high withstand voltage and reliability is provided since the generation of hot carriers can be prevented by the second base layer 4. (see image in original document) (see image in original document)

...SPECIFICATION voltage MIS field effect transistors. The high withstand voltage MIS field effect transistor shown in Fig. 19 is a MOSFET produced by the double diffusion **process** and is called a vertical DMOS since the current just under the gate is caused to flow in a vertical direction in a semiconductor substrate. The high withstand voltage MIS field effect transistor shown in Fig. 20 is a MOSFET produced by the same double diffusion **process** as in Fig. 19 and is called a horizontal DMOS since the current just under the gate is caused to flow in a transverse direction...

...reverse bias voltage is applied in the vertical DMOS, a depletion layer is extended in the vertical direction. To maintain a sufficient withstand voltage, the **impurity** concentration of the epi layer 20 should be lowered and the thickness thereof should be sufficient.

On the other hand, a horizontal DMOS (Fig. 20...

...of a power MOSFET, which has a large area in a power IC, is important. When the power MOSFET portion is produced, if the production **process** is increased, reduction of the production cost is difficult, if not impossible.

In the conventional vertical DMOS described above, a adequate thickness is needed to...said MIS portion and said drain portion. A semi-insulating layer is disposed through an insulating film over said region.

The present invention has been **made** in view of the above circumstances and has as an object a high withstand voltage MIS field effect transistor which realizes the merits of the...

...lower substrate and the upper second base layer in this well region and the current path is interrupted by the JFET effect even in this **well** region. Consequently, a **high** withstand **voltage** property can even be maintained in the well region with the lateral length, and there is no need for a well region length that raises the

problem of increased resistance in the horizontal DMOS. Since the **impurity** concentration of the substrate is low, when the width of the depletion layer is **made** uniform by decreasing the **impurity** concentration of the second base layer more than in the first base layer, the JFET effect can be efficiently obtained in this region.
Further, since...

...at the same time. Thus, in the one chip semiconductor integrated circuit device using the high withstand voltage MOSFET 31 of the present example, a **high** withstand voltage **well** and a **low voltage** withstand **well** for a control circuit portion can be formed at the same time and the time chip production **process** can be shortened.

...base layer 3 and the well layer 2 and from the PN junction portion between the silicon substrate 1 and the well layer 2. Since **impurity** concentration in the well layer 2 and the substrate 1 is low, a depletion layer is increasingly extended to these regions. When a reverse bias...path can be blocked, as in the JFET, thereby obtaining a high withstand voltage. Since a desired withstand voltage can be obtained even if the **impurity** concentration is increased, a low resistance during operation can be realized by increasing the **impurity** concentration. As described above, in the MOSFET according to the present example, a **high** withstand **voltage** as **well** as a low resistance can be realized. Of course, a leak current is not generated in the surface of the well layer as in the...

...between the offset layers 42.1 to 42.3. For example, if the well layer 2 is formed by a thermal diffusion after an ion **implantation,** the **impurity** concentration is the highest in the well layer 2 surface. Thus, by forming the island shaped offset layer, the high concentration surface can be left and the **impurity** concentration of the entire well layer 2 is high and the resistance value of the well layer 2 is decreased. Thus, by forming the offset...

...42.3 a high withstand and a low resistance MOSFET can be formed. In a case where the well layer 2 is formed without ion **implantation,** even if, for ...in the MOSFET of the present example, a low resistance can be realized by the JFET effect as explained in the example 5 and the **impurity** concentration can be increased so that a high withstand and low resistance MOSFET can be realized. When a reverse bias is applied, depletion layers are...

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/15 (Item 15 from file: 348)
DIALOG(R)File 348:**EUROPEAN PATENTS**

Low voltage device in a high voltage substrate
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PATENT (CC, No, Kind, Date): EP 478123 A1 920401 (Basic)
EP 478123 B1 960925
APPLICATION (CC, No, Date): EP 91306667 910722;

PRIORITY (CC, No, Date): US 590277 900928

ABSTRACT EP 478123 A1

A semiconductor substrate of a first conductivity type includes a well structure of a second conductivity type formed therein. A first low voltage MOS transistor includes spaced apart source and drain regions of the first conductivity type in the well. A first transistor gate lies above a channel region which is disposed between the source and drain regions of the first low voltage MOS transistor and is separated therefrom by a gate **dielectric** having a first thickness. A **second** high voltage transistor includes spaced apart source and drain regions of the first conductivity type in the well. A second transistor gate lies above a channel region which is disposed between the source and drain regions of the second high voltage transistor and is separated therefrom by a gate **dielectric** having a **second** thickness which is greater than the thickness of the gate dielectric of the first low voltage MOS transistor. A first contact diffusion, having the same conductivity type as the well, is located at the edge of the well closest to the first low voltage transistor, and is connected to a source of voltage. A second contact diffusion, having the same conductivity type as the well, is located at the edge of the well closest to the second high voltage transistor, and is also connected to the source of voltage. (see image in original document)

...SPECIFICATION A1

...the PROM. The design of MOSFET or MESFET circuits which include an interface between low voltage circuits and high voltage circuits traditionally incorporates two separate **wells,** one **well** for **low voltage** devices and a second **well** for **high voltage** devices. These separate **wells** are usually surrounded by double guard rings to suppress destructive latch up. The double wells and their attendant guard rings constitute a considerable layout area...

...channel region which is disposed between the source and drain regions of the first low voltage MOS transistor and is separated therefrom by a gate **dielectric** having a first thickness.

A **second** high voltage transistor includes spaced apart source and drain regions of the first conductivity type in the well. A second transistor gate lies above a channel region which is disposed between the source and drain regions of the second high voltage transistor and is separated therefrom by a gate **dielectric** having a **second** thickness which is greater than the thickness of the gate dielectric of the first low voltage MOS transistor.

A first contact diffusion, having the same...

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/16 (Item 16 from file: 348)

DIALOG(R)File 348:**EUROPEAN PATENTS**

Process for forming high-voltage and low-voltage CMOS transistors on a single integrated circuit chip

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PATENT (CC, No, Kind, Date): EP 387999 A2 900919 (Basic)
EP 387999 A3 920729
EP 387999 B1 981104
APPLICATION (CC, No, Date): EP 90301381 900209;
PRIORITY (CC, No, Date): US 324869 890317

ABSTRACT EP 387999 A2

A **process** for forming both low-voltage CMOS transistors and high-voltage CMOS transistors on a common integrated circuit chip uses a common **implantation** and drive-in step to form both the n-type well (174,374) of each PMOS transistor and the n-type drain extension well (274) of each lightly-doped drain (LDD) NMOS transistor and a separate **implant** and drive-in to form the p-type drain extension well (182) of each LDD PMOS transistor. (see image in original document)

...SPECIFICATION 1986).

Summary of the Invention

A **process** according to the present invention is characterised by the features specified in claim 1.

The present invention is directed to a **process** for providing both high-voltage and low-voltage CMOS devices in a common chip that basically involves adding a single ion **implantation** step, some non-critical masking and mask design changes to an established n-type **well, low-voltage** CMOS integrated circuit **process.**

In particular, early in this novel **process**, the mask that is characteristically used with the standard donor ion **implantation** step for forming in a p-type substrate n-type wells for the p-channel (PMOS) transistors is modified additionally to form extension n-type **wells** for the **high-voltage** n-channel (NMOS) transistors. Additionally, the novel **process** includes an added acceptor ion **implantation** step for forming p-type wells for use in forming the high-voltage PMOS transistors. In particular, the parameters of the **implantation** step that forms the p-type extension well permits the standard field oxidation step to be used to drive-in the **implanted** ions.

Moreover, in a preferred embodiment for achieving additionally a thicker gate oxide layer in each of the high-voltage transistors, at an intermediate stage in the **process**, a mask used for localizing an oxide-**etching** step is modified to protect the oxide in the active region of each high-voltage transistor so that ultimately the gate oxide layer of each...

CLAIMS

2. A **process** according to claim 1, whereby the step of growing an oxide layer between the thick field oxide regions comprises the steps of growing a first oxide layer (88) between the thick field oxide regions; **removing** the first oxide layer (88) selectively where the gates of the low-voltage transistors are to be formed; and then growing a **second oxide** layer (389,489) where the first

oxide layer was **removed** whilst simultaneously thickening the first oxide layer (189,289) where the gates of the high-voltage transistors are to be formed.

3. A **process** according to claim 1 or claim 2, wherein the drain extension **well** (274) of each **high-voltage** transistors of the opposite conductivity type is formed by **implantation** and drive-in steps that simultaneously form the wells (174,374) of the transistors of said one conductivity type.
4. A **process** as claimed in any one of claims 1 to 3, wherein said one conductivity type is p-type and said other conductivity type is n-type.
5. A **process** as claimed in claim 4, wherein the drain of each high-voltage transistor of said one conductivity type is formed by **implanting** acceptor ions within selected regions of each drain extension **well** (182) of each **high-voltage** transistor of said one conductivity type to form heavily doped drain regions (190) whilst simultaneously **implanting** acceptor ions into selected regions of the **wells** (174) of each **high-voltage** transistor of said one conductivity type to form the source (192) of said high-voltage transistor and into selected regions of the **wells** (374) of each **low-voltage** transistor of said one conductivity type to form the drain (392) and the source (390) of the low-voltage transistor of said one conductivity type.
6. A **process** as claimed in claim 4, wherein the drain of each high-voltage transistor of said other conductivity type is formed by **implanting** donor ions within selected regions of each drain extension **well** (274) of each **high-voltage** transistor of said other conductivity type to form heavily doped drain regions (290) whilst simultaneously **implanting** donor ions into selected regions of the substrate (12) to form the source (292) of each high-voltage transistor of said other conductivity type and the drain (490) and the source (492) of the low-voltage transistor of said other conductivity type.
7. A **process** as claimed in any one of claims 1 to 7, wherein the gates (196,296,396,496) of the transistors are formed by providing a doped polysilicon layer on selected areas of the substrate (12) covered by the oxide layer (189,289,389,489).
8. A **process** of forming in a common substrate (12) an integrated circuit that includes both low-voltage CMOS transistors and high-voltage CMOS transistors of the LDD type, said **process** comprising the steps of forming at a surface (12a) of a p-type substrate (12) a non-uniform layer of silicon oxide having thick portions...

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/21 (Item 21 from file: 349)

INTEGRATION OF HIGH VOLTAGE SELF-ALIGNED MOS COMPONENTS

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Patent and Priority Information (Country, Number, Date):

Patent: **WO 200237547 A1 20020510** (WO 0237547)
Application: WO 2001SE2405 20011101 (PCT/WO SE0102405)

English Abstract
The invention relates to a **method** for forming a high voltage NMOS transistor together with a low voltage NMOS transistor and a low voltage PMOS transistor, respectively, in an n-well CMOS **process** by adding solely two additional **process** steps to a conventional CMOS **process**: (i) a masking step, and (ii) an ion **implantation** step for forming a doped channel region (31) for the high voltage MOS transistor in the substrate (1) self-aligned to the edge of the high voltage MOS transistor gate region (25). The ion **implantation** (35) is performed through the mask (33) in a direction, which is inclined at an angle (a) to the normal of the substrate surface, to...

SUMMARY OF THE INVENTION

These objects among others are,, according to one aspect of the invention, fulfilled by a **method** wherein a semiconductor substrate is provided; n-**well** regions for the **high voltage** NMOS transistor and the low voltage PMOS transistor are formed in the substrate by means of ion **implantation**; a p-**well** region for the **low voltage** NMOS transistor is formed in the substrate by means of ion **implantation**; and isolation areas are formed on top of and/or in the substrate to laterally separate the transistor from each other and to define a...

According to yet a further aspect of the invention a **method** for forming a high voltage NMOS transistor together with a low voltage NMOS transistor in a MOS **process** (e.g. CMOS, BiCMOS, or NMOS **process**) comprising the steps of providing a semiconductor substrate; forming n-**well** regions for the **high voltage** NMOS transistor in the substrate by means of ion **implantation**; forming a p **well** region for the **low voltage** NMOS transistor in the substrate by means of ion **implantation**; forming isolation areas on top of and/or in the substrate to laterally separate the transistors from each other and to define a voltage distributing...

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9/TI,PN,AU,IN,PD,AN,AD,AB,K/23 (Item 23 from file: 349)
DIALOG(R)File 349:**PCT FULLTEXT**

A HIGH VOLTAGE TRANSISTOR HAVING A FIELD OXIDE GATE REGION
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English Abstract

A high voltage transistor, formed in a bulk semiconductor material (200), has a gate region (230) defined by a relatively thick field oxide (205) and a source (220) and drain (225) on opposite sides of the field oxide (205).

Detailed Description

For additional isolation between the **low** and **high** **voltage** devices a p-**well** block can be constructed (step 115). The p-well block does not require an additional **process** step (e.g., **implantation**), but rather a change in existing **low** **voltage** device p-**well** masking to ensure a physical separation between **low** voltage device p-**wells** and adjacent **high** **voltage** device n-**wells**. Thus, p-well blocks are formed during **low voltage** device p-**well** formation at no additional **process** cost. The p-well block ensures there are three distinct regions at the surface of the substrate: p-well; n-well; and bulk. The electrically...

...regions (i.e., the bulk regions are not used to set any electrical characteristic of the low voltage devices) enable formation of useful and stable **high voltage** devices.

P-**well** block formation (step 115) is followed by a relatively short and low temperature anneal phase designed to activate the **implantation** regions (step 120). A typical activation anneal uses an 850C to 1000C bake for 15 to 60 minutes. The anneal's relatively low temperature and short time period limits the lateral diffusion of the **implanted** ions, resulting in relatively sharp well edges and well ionic concentration of approximately 1eI6 to 5eII ions/cm'.

Referring to FIGs. 4 and 5, an alternative embodiment is shown which uses an additional mask to **expose** the high voltage device gate oxide region (step 5) and a timed **etch** (step 405) to selectively reduce the gate oxide's thickness 500. With the addition of this one operation (one mask to **open** a photoresist **window** over the high voltage device's gate oxide and one **etch**), the drive capacity of the high voltage device may be increased approximately five times without affecting low voltage device characteristics. The **etch** (step 405) may be performed, for example, by a timed buffered oxide **etch** (BOE) or buffered hydrofluoric acid (HF) **etch**. The precise time of the **etch** depends at least upon the gate oxide's initial thickness and concentration of the **etchant** (e.g., HF). The gate oxide 500 may be taken as thin as desired (within control limits of the timed **etch**), typically 400A to 1000A. The effect of this operation is to increase high voltage device transconductance which, also has the effect of reducing the high...

...This embodiment retains all of the advantages, and can be modified in the same manner, as the prior embodiment while incurring only a minimal added **fabrication** cost.

Referring to FIGs. 6 and 7, the prior embodiment is modified to provide a high voltage device gate **implantation** step (600) after the gate oxide has been **exposed** (step 400) but before it has been **etched** (step 405). **Implant** energies may be between approximately le" to le" ions/cM2, generally using B or boron-fluoride (BF2)ions. Shallow **implantation** energies of approximately 100 KeV to 200 KeV, and deep **implantation** energies of approximately 100 KeV to 1 MeV may be used. Gate region **implantation** may also be performed before the gate **etch** (step 405) and, if so, **implantation** energies as low as 25 KeV for a shallow **implant**, and 300 KeV for a deep **implant** may be used. If the modified p-type gate material 710 is annealed at the same time the source and drain regions are annealed (step 120), no additional **processing** is necessary. Gate region **implantation** (step 600 and region 705) can allow the high voltage device source and drain regions to be more closely spaced which, in turn, tends to reduce the effect of the device's channel length and increases the high voltage device's current drive capability. **Implantation** (step 600) also allows an increased flexibility in setting the high voltage device's electrical characteristics, such as its threshold voltage.